What is claimed is:

1. A communications interface, comprising:
a bus interface coupleable to a bus;
a plurality of transmit channels coupled to the bus interface;
a transmit control block coupled to the plurality of transmit channels;
a plurality of receive channels coupled to the bus interface; and
a receive control block coupled to the plurality of receive control channels.

2. The communications interface of claim 1, further comprising a direct memory access controller coupled to the bus interface.

3. The communications interface of claim 1, wherein the bus interface comprises a plurality of transmit control registers and a plurality of receive control registers.

4. The communications interface of claim 3, wherein the plurality of transmit control registers comprises at least one of:
an interface width register coupled to the transmit control block;
a transmit first in first out (FIFO) register associated with each transmit channel;
an end of message (EOM) register associated with each transmit channel;
an interface interrupt identification register coupled to the transmit control block;
a transmit frequency select register coupled to the transmit control block;
a wait count register coupled to the transmit control block;
a clock stop time register coupled to the transmit control block;
a channel configuration register associated with each transmit channel; and
a channel status register associated with each transmit channel.

5. The communications interface of claim 3, wherein the plurality of receive control registers comprises at least one of:

a receive FIFO register coupled to each receive channel;

an interface width register to select a predetermined number of bits to be received across the communications interface by the receive control block;

a channel stop register associated with each receive channel;

a channel start register associated with each receive channel;

a wake up register associated with at least one receive channel;

an end of message register associated with each receive channel;

a channel configuration register associated with each receive channel; and

a channel status register associated with each receive channel.

6. The communications interface of claim 1, wherein each of the plurality of transmit channels and each of the plurality of receive channels comprises a first in first out (FIFO) memory device.

7. The communications interface of claim 1, further comprising a power management unit coupled to each of the plurality of transmit channels and receive channels.

8. The communications interface of claim 1, wherein the transmit control block comprises a channel arbiter adapted to select a next one of the plurality of transmit channels to be activated.

9. The communications interface of claim 1, wherein the transmit control block comprises a link controller adapted to transmit data from a selected transmit channel across a selected link.

10. The communications interface of claim 1, wherein the receive control block comprises a state machine adapted to store a current active channel number, a number of bits in a current byte being transferred and to write each byte to a selected one of the plurality of receive channels.

11. The communications interface of claim 1, wherein the plurality of transmit channels comprises:

at least one channel adapted to send a clock signal;

at least one channel adapted to send a strobe signal;

at least one channel adapted to send a wait signal; and

at least one channel adapted to send data.

12. The communications interface of claim 1, wherein the plurality of receive channels comprises:

at least one channel adapted to send a clock signal;

at least one channel adapted to send a strobe signal;

at least one channel adapted to send a wait signal; and

at least one channel adapted to send data.

13. The communications interface of claim 1, wherein at least one of the plurality of transmit channels and the plurality of receive channels comprise a virtual general purpose input/output channel.

14. The communications interface of claim 1, further comprising:

a channel stop threshold register adapted to set a threshold value to cause a stop message to be sent to a source when a receive FIFO is full; and

a start threshold register adapted to set a start threshold value to cause a start message to be sent to a source when the receive FIFO can receive additional data.

15. The communications interface claim 1, further comprising:

a stop message channel coupled to the receive control block and adapted to send a stop message to a source when a receive FIFO reaches a stop threshold value; and

a start message channel coupled to the receive control block and adapted to send a start message to the source when the receive FIFO reaches a start threshold value.

16. The communications interface of claim 1, further comprising at least one of a direct flow control mode and a message flow control to control a flow of data across the communications interface.

17. The communications interface of claim 1, wherein the transmit control block comprises:

a multiplexer coupled to the plurality of transmit channels;

a parallel in serial out converter (PISO) coupled to the multiplexer; and

a control circuit coupled to the multiplexer and the PISO and adapted to select one of the plurality of transmit channels to transmit data.

18. The communications interface of claim 1, wherein the receive control block comprises:

a demultiplexer coupled to the plurality of receive channels;

a serial in parallel out converter (SIPO); and

a control circuit coupled to the demultiplexer and adapted to select one of the plurality of receive channels to receive data.

19. An electronic system, comprising:

a first semiconductor chip;

a first communications interface coupled to the first semiconductor chip;

a second communications interface coupled to the first communications interface, wherein each of the first and second communications interfaces include:

a bus interface coupled to the first semiconductor chip,

a plurality of transmit channels coupled to the bus interface,

a transmit control block coupled to the plurality of transmit channels,

a plurality of receive channels coupled to the bus interface, and

a receive control block coupled to the plurality of receive control channels; and

a second semiconductor chip coupled to the second communications interface.

20. The electronic system of claim 19, further comprising at least one of a direct flow control mode and a message flow control mode to control the flow of data between the first chip and the second chip.

21. The electronic system of claim 19, wherein at least one of the first or second semiconductor chips is a memory device and further comprising a direct memory access controller coupled to between the memory device and the bus interface.

22. The electronic system of claim 19, wherein the transmit control block comprises a channel arbiter adapted to select a next one of the plurality of transmit channels to be activated.

23. The electronic system of claim 19, wherein the transmit control block comprises a link controller adapted to transmit data from a selected transmit channel to one of the first or second semiconductor chips.

24. The electronic system of claim 19, wherein the receive control block comprises a state machine adapted to store a currently active channel number, a number of bits in a current byte being transferred and to write each byte to a selected one of the plurality of receive channels.

25. The electronic system of claim 19, wherein each of the plurality of transmit channels and each of the plurality of receive channels comprises:

at least one channel adapted to send a clock signal;

at least one channel adapted to send a strobe signal;

at least one channel adapted to send a wait signal; and

at least one channel adapted to send data.

26. The electronic system of claim 19, wherein at least one of the plurality of transmit channels and one of the plurality of receive channels comprise a virtual general purpose input/output channel.

27. The electronic system of claim 19, further comprising:

a stop message channel coupled to the bus interface and adapted to send a stop message to one of the first or the second semiconductor chips when a receive FIFO reaches a stop threshold value; and

a start message channel coupled to the bus interface and adapted to send a start message to the other of the first or the second semiconductor chips when the receive FIFO reaches a start threshold value.

28. A method of transmitting data between semiconductor chips, comprising:

writing data into at least one of a plurality of transmit FIFOs;

selecting one of the plurality of transmit FIFOs that contains data to be transmitted and that is not in a wait state; and

transmitting the data to a corresponding one of the plurality of receive FIFOs that has not exceeded a threshold value.

29. The method of claim 28, further comprising:

sending a wait signal to a transmit control block if the corresponding one of the receive FIFOs cannot receive data; and

removing the wait signal when the corresponding one of the receive FIFOs can receive data.

30. The method of claim 28, further comprising selecting another one of the plurality of transmit FIFOs to send data to another corresponding one of the plurality of receive FIFOs while the corresponding one of the receive FIFOs cannot receive data.

31. The method of claim 28, further comprising:

sending a strobe signal to initiate a transmission of data;

sending a selected channel number over which the data is to be transmitted; and

sending an end of message signal after the data has been transmitted.

32. The method of claim 28, further comprising:

sending a stop message if the corresponding one of the receive FIFOs cannot receive data; and

sending a start message when the corresponding one of the receive FIFOs can receive data.

33. The method of claim 28, further comprising:

selecting one of the plurality of transmit FIFOs and the corresponding one of the plurality of receive FIFOs by a predetermined algorithm.

34. The method of claim 28, wherein the predetermined algorithm is round-robin.

35. The method of claim 28, further comprising selecting a interface width from one of a serial width, a two-bit width and a nibble width.

36. A method of forming a communications interface, comprising:

forming a bus interface;

forming a plurality of transmit channels coupled to the bus interface;

forming a transmit control block coupled to the plurality of transmit channels;

forming a plurality of receive channels coupled to the bus interface; and

forming a receive control block coupled to the plurality of receive control channels.

37. The method of claim 36, wherein forming the bus interface comprises forming a plurality of transmit control registers and a plurality of receive control registers.

38. The method of claim 36, wherein forming the transmit control block comprises:

forming a channel arbiter adapted to determine a next one of the plurality of channels to be activated; and

forming a link controller adapted to transmit data from a selected transmit channel across a selected link.

39. The method of claim 36, wherein forming the receive control block comprises forming a state machine adapted to store a currently active channel number, a number of bits in a current byte being transferred and to write each byte to a selected one of the plurality of receive channels.

40. The method of claim 36, wherein forming the plurality of transmit channels and forming the plurality of receive channels, each comprises:

forming at least one channel adapted to send a clock signal;

forming at least one channel adapted to send a strobe signal;

forming at least one channel adapted to send a wait signal; and

forming at least one channel adapted to send data.

41. The method of claim 36, further comprising forming at least one virtual general purpose input/output channel.

42. The method of claim 36, wherein forming the transmit control block comprises:

forming a multiplexer coupled to the plurality of transmit channels;

forming a parallel in serial out converter (PISO) coupled to the multiplexer; and

forming a control circuit coupled to the multiplexer and to the PISO.

43. The method of claim 36, wherein forming the receipt control block comprises:

forming a demultiplexer coupled to the plurality of receive channels;

forming a serial in parallel out converter (SIPO);

forming a control circuit coupled to the demultiplexer and adapted to select one of the plurality of receive channels to receive data.